Research Center for Photovoltaics

シリコンヘテロ接合太陽電池の界面欠陥の評価

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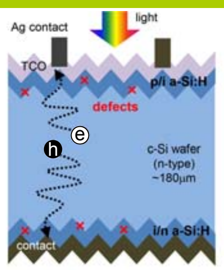
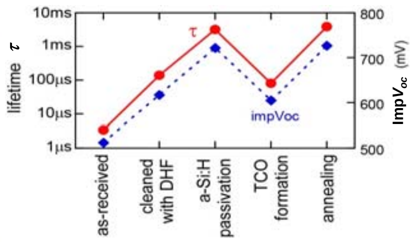
Abstract

- **Defect kinetics** in **a-Si:H/c-Si heterojunction** is studied throughout fabrication process, particularly during a-Si:H growth.
- During a-Si:H growth, defects are generated not only in an **a-Si:H layer** but also **c-Si bulk**.
- The defects in a-Si:H are recovered completely by postannealing, whereas defects in c-Si are partially recovered by postannealing. The **residual defects** are formed in c-Si.
- The **a-Si:H/c-Si interface defects** are formed by postannealing.

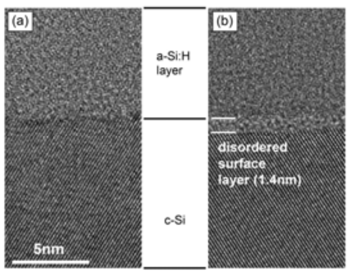
SHJ solar cell structure & minority carrier lifetime





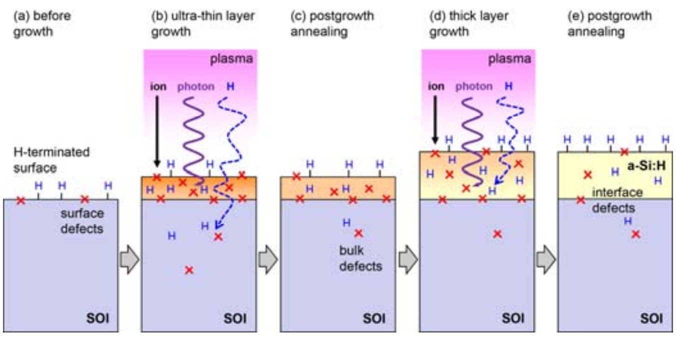
- In SHJ solar cells, a-Si:H layer plays important roles in surface passivation & carrier selection.
- The lifetime, i.e., a measure for the surface passivation, varies throughout the fabrication process of SHJ solar cells

TEM analysis for a-S:H/c-Si interface



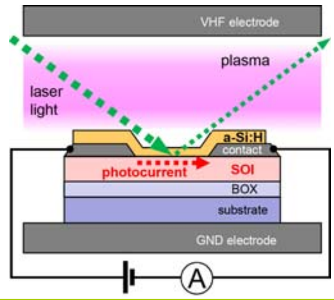
- (a) **Sharp interface of a-Si:H/SOI stack**. The a-Si:H layer is grown over the SOI by SiH_4/H_2 discharges at 147 °C for 60 s, yielding the thickness of 18.0 nm.
- (b) **a-Si:H/SOI interface** with **disordered surface layer (DSL)**. The DSL (≈1.3 nm) is created by a H_2 plasma treatment for 100 s, before a-Si:H growth.

Model: defect kinetics in a-Si:H/c-Si



Defect kinetics in a-Si:H/c-Si stack. *(a) Before a-Si:H growth*. The DHF-treated SOI surface is terminated with H atoms. *(b) Ultra-thin layer growth*. The **defects are generated both in the a-Si:H and the SOI** by energetic and/or reactive species of radicals, ions and photons coming from plasma. The **bulk defects in the SOI** are generated in this stage. *(c) Postannealing*. The defects in the a-Si:H and the SOI are annihilated. However, a large amount of defects remain in an ultra-thin layer. *(d) Thick layer growth*. The defects are generated mainly in the a-Si:H layer. *(e) Postannealing*. The defects in the a-Si:H layer are annihilated, yielding the surface passivation. A small amount of **the interface defects** are created by postannealing.

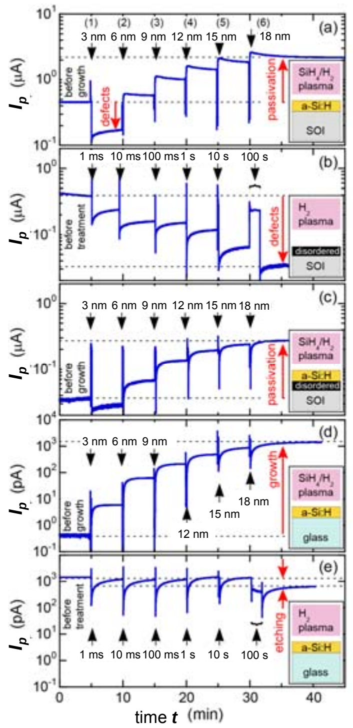
Exp. Setup: In-situ real-time photocurrent measurement



- **Silicon on insulator (SOI)** is used as a sample for the photocurrent measurement.
- SOI is illuminated with a **semiconductor laser** (520 nm, 1 mW) during a-Si:H growth.
- The **photocurrent** is measured during a-Si:H growth and also subsequent postannealing.
- In experiments, **the growth time (Δt), i.e., the thickness of a-Si:H passivation layer** is varied.

Experimental results

Time evolution of photocurrents



- **(a) a-Si:H growth over SOI.** I_p is increased with the number of growth, i.e., the layer thickness, except for the first growth of an ultra-thin layer. The increase in I_p means the termination of defects over the SOI surface, i.e., the surface passivation.
- **(b) H_2 plasma treatments of SOI.** Each treatment causes a reduction in I_p, indicating the generation of defects in the SOI. The reduction is enhanced for a long-time treatment.
- **(c) a-Si:H growth over SOI with DSL.** The surface passivation is recognized even for the SOI surface with DSL.
- **(d) a-Si:H growth over glass substrate.** I_p is significantly increased with the number of growth.
- **(e) H_2 plasma treatments of sole a-Si:H over glass.** Each treatment causes a reduction in I_p, indicating the generation of defects. During postannealing, I_p returns completely to the initial level, i.e, defect recovery.

S. Nunomura *et al.*, *Appl. Phys. Express* **12**, 051006 (2019).
S. Nunomura *et al.*, *AIP Advances* **9**, 045110 (2019).

Summary

- **The defect kinetics in the a-Si:H/SOI stack is studied via in-situ photocurrent measurements.**
- During growth, the defects are generated mainly in the a-Si:H layer. However, these defects are recovered completely by postannealing.
- The **bulk defects in the SOI** are generated by the penetration of H atoms, which is demonstrated by the experiments of the SOI treated with H_2 plasmas. These defects are partially recovered by postannealing; most of the defects remain in the SOI, which deteriorates the passivation quality.
- During postannealing, **the interface defects** are created in the a-Si:H/SOI. The suppression of these interface defects as well as the bulk defects in the SOI, i.e., c-Si, is crucial for high-quality and reliable passivation.

Acknowledgements

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