IEC standardization of BD Thermal Runaway Test (IEC62979CD / Doc. 82/1025/CD)

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IEC standardization of BD Thermal Runaway Test

1. Proposed background

2. Test conditions of “Thermal Runaway Test”

3. Current situation of “IEC standardization”

4. Another effort (Tj measurement)

5. Acknowledgement
Quality Assurance Forum in order to establish the high reliability PV module started on July 2011 in San-Francisco US.

TG-1 ; PV QA Guideline for Manufacturing Consistency

TG-2 ; Thermal and Mechanical fatigue including vibration

TG-3 ; Humidity, Temperature and Voltage

TG-4 ; Diode, Shading & Reverse bias / Leader Dr. Paul Robust
        Dr. Vivek Gade

TG-5 ; UV, Temperature and Humidity
Progress


Oct., 2014 NP/New work item Proposal was approved.
Participation: US, DE, CN, CR, JP

Sep., 2015 WD/Working Draft was proposed.
Circulated CD for 3 months.

Dec., 2015 Received 44 comments from CN, DE, NL, PT, US
Technical 23, Editorial 15, General 6

Feb., 2016 Participated in NREL Reliability PV Module Workshop
“Behavior of BD during Thermal Runaway Test”

May, 2016 WG2 Taipei meeting
Discussion about test conditions and pass criteria.

Jun. 15, 2016 sent the CDV draft to WG2 convener.

Aug. 26, 2016 CD voting is been circulating until 18 Nov. 2016.
In many cases, Bypass Diode (BD) P/N diode

IEC61215 Ed.1

IEC61215 Ed.2 (2005/April)

SBD (Schottky Barrier Diode)

⇒ The demerit of SBD is a low withstanding of reverse voltage at the high temperature.
• In order to satisfy the requirements of “10.18 Bypass diode thermal test” in IEC61215 Ed.2, the bypass diode has been switched to the SBD with low Vf.

• However, the breakdown voltage of the reverse bias at high temperature of the SBD as compared with Si P/N diode is low.

• Therefore, we have to verify the thermal design by the thermal runaway test.
The need for the thermal runaway test

- When the PV module’s surface is in the shade (ex.: shade by the protuberance such as utility poles, buildings, and/or leaves) during a sunny irradiation condition, the current flows to the bypass diode (BD) in the J-box through the cell-string.
- Under these circumstances, the temperature of the BD increases after a certain period of time.
- If the shade suddenly disappears, the reverse bias voltage from the cell’s string is applied to the BD.
- In the situation where thermal runaway might occur after the increasing of the diode leak-current, when the BD which has the low withstanding reverse voltage at high temperature is used.
- Therefore, the thermal design of the BD in the J-box should be verified with the thermal runaway test.
Presented at NREL work-shop 2012

Typical SBD

Typical Si P/N diode

Graph 1: Reverse bias (V) vs Temperature (°C)

Graph 2: Reverse bias (V) vs Temperature (°C)
Destructive analysis of the diode of leakage state by thermal-runaway

Appearance of Thermal-runaway diode → No problem

X-ray image → No problem

Image to removed the resin

The property was in a short state.

Melting traces of chip → Typical failure pattern by thermal runaway

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Test conditions</th>
<th>Measured value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VFM</td>
<td>0.58V(max)</td>
<td>25°C, 30A</td>
<td>0.51V</td>
</tr>
<tr>
<td>VRM</td>
<td>45V(min)</td>
<td>25°C, 1mA</td>
<td>Short</td>
</tr>
</tbody>
</table>
Five items to be discussed

1. Module temperature - Approved
2. Test conditions of applying of forward current - Approved
3. Switching over time to reverse bias voltage - Approved
4. Pass criteria - Modified
5. Test target of P/N diode - Approved
Test procedure of Thermal runaway test

1. Measurement of initial Ir (reverse current)
2. Apply a forward current to BD at 75°C or 90°C.
3. Apply a reverse bias voltage to BD within 10ms after disconnection of forward current.
4. Measurement of Ir after testing
2-1 Module temperature

a) 75°C for Open-rack

b) 90°C for Roof-mount

Based on the outdoor exposure data of NEDO project, 90°C was proposed as the temperature of the roof-mount. After that, 75°C was added as temperature for the open-mount.
The test condition “90°C” is proposed assuming the worst case according to the following results.

Sample of the PV module temperature recorded at the top 5 sites selected from 47 sites in Japan.

Selected data >>> 2003/1/1 to 2013/1/1 for 10 years
2-2 Applying of forward current

a) Forward current
   1.25 X Isc (A) of PV module
   ➔ Followed the test conditions of “Bypass Diode Thermal Test”.

b) Applying time
   Apply the forward current of the BD for at least 40 minutes and until the range of Tlead change during 10 minutes becomes within 0.3°C.
2–3 Applying of reverse voltage

Shut-off the forward current. Within 10 ms, apply the reverse bias voltage to the BD to be tested.
To verify the effect of the switching time, the energy immediately after the reverse bias voltage application was measured by changing of the switching time.

\[ Pf (W) = \text{Forward direction energy just before applying of reverse bias voltage.} \]

\[ Pr (W) = \text{Energy immediately after reverse bias voltage was applied.} \]
The effect of Switching over time

With the increase of the switching over time (from 5ms to 200ms), the value of Pr becomes smaller.

This means, Tj will decrease if a longer switching over time is applied.

The proposed 10ms is considered reasonable and is obtainable by PC controller.
Are switch over times of 10 ms realistic? / Comment ; DE07

4.5 Test procedure  c)

Field measurements in real system are desirable.

Outdoor measurements were performed.

→ The switching time of 15 ms to 24 ms were obtained (or measured).

Based on the above results, the test condition of 10 ms is proposed.

This test condition is achievable by using a high speed response relay.

<table>
<thead>
<tr>
<th>Position of shading</th>
<th>Switch over time, N=4</th>
</tr>
</thead>
<tbody>
<tr>
<td>① Left side cluster</td>
<td>20 ~ 24 ms</td>
</tr>
<tr>
<td>② Center cluster</td>
<td>15 ~ 21 ms</td>
</tr>
<tr>
<td>③ Right side cluster</td>
<td>15 ~ 20 ms</td>
</tr>
</tbody>
</table>

→ Make shading on a cell by cardboard with thread, shading was cleared by removing the cardboard quickly by hand.
2-4 Pass or Fail criteria

a) In case that Tlead and leakage current decrease, and if the reverse leakage current at -10V after the test does not increase to more than 5 times of the initial value, the BD is considered safe from the possibility of thermal runaway and pass the test.

→ Tlead, Ir が逆バイアス印加後減少し、Irが初期値に対して、5倍以内であれば合格

b) In other case, namely if Tlead and leakage current increase or if the reverse leakage current at -10V after the test increase to more than 5 times of the initial value, the BD is considered to have failed.

→ Tlead, Ir が逆バイアス印加後増加し、Irが初期値に対して、5倍以上であれば不合格
Tlead and leakage current during thermal runaway

Tlead observation is not considered suitable for the evaluation of thermal runaway phenomenon.
To cope with these difficulties, the observation of leakage current is recommended as an effective method. The leakage current respond sharply to thermal runaway.

熱暴走時のTleadによる温度上昇は緩やかであるが、漏れ電流のそれは素早く上昇する。
In case of thermal runaway occurrence, $I_r$ becomes large leakage current.

The reverse characteristic after thermal runaway shows obvious changes.
The test specimen which employs P/N diodes as bypass diode could be exempted from the thermal runaway test required herein, because the capacity of P/N diodes to withstand the reverse bias is sufficiently high.

P/N diode は、高温逆耐圧が SBD (Schottky Barrier Diode) に比べ十分高いため、この試験の対象から除く。
Foundation data

P/N diodes’ capability to withstand the reverse voltage at the high temperature is very high (about one thousand volts).

P/N diode could be exempted from the required thermal runaway test, because its capability to withstand the reverse bias voltage is high enough.

Typical SBD

Typical Si P/N diode

Presented at NREL work-shop 2012
Discussion of Thermal runaway test

19 May, 2016
TC82/WG2 members of the Taipei meeting, which was held in May 2016.
Current situation of IEC standardization

1. NP / New work item Proposal finished
2. 3 months vote finished
3. WD / Working Draft finished
4. CD >>> 3 months comments
   Sep. 11 ~ Dec. 11, 2015 circulating
   sent CDV draft to WG2 convener in 15 Jun. 2016
5. CDV >>> 12 weeks vote
   Agreement of P-members > 2/3
   Negative vote < ¼ of total vote
   Circulating Aug. 26 – Closing date Nov. 18
6. FDIS preparation by organizer
7. FDIS preparation by CO CO (Central office)
8. FDIS 8 weeks vote CO
9. IS / International standard CO
As the Tj measurement method for Bypass diode,

10.18.3 Procedure 1 → Tlead / case method
In the case of Tlead/case method, we should consider "10C margin". The test results showed that about 10°C difference may exist between the calculated Tj by “Tlead method” and the real Tj (Tj measured by Vf-Tj method).
This difference could not be overlooked. It is considered appropriate to revise the pass criteria of the test to have 10°C margin to the diode manufacturer’s maximum junction temperature rating in the case of the “Tlead method” is used.

10.18.4 Procedure 2 → Vf-Tj method
JET would like to be unified to Vf-Tj method, because it is a primary method for Tj measurement.
The relation between $T_j$ and $T_{lead}$ is expressed as below using the parameter of thermal resistance ($R_{th}$).

$$T_j = T_{lead} + (V_f \times I_f \times R_{th})$$

The value of $R_{th}$ is usually supplied by the diode manufacturer.

The problem is that the value supplied is not a real $R_{th}$, but an apparent value of $R_{th}$ which will vary according to the heat dissipating condition where the diode is installed. (see next slide)
Thermal resistance varies by the difference of heat dissipating condition such as a J-box.

Thermal source (Diode junction) \( P = V_f \times I_f \)

Apparent \( R_{th} \) will vary according to the heat flow ratio which varies with the radiation condition of each route !!!!!

\[
T_j = T_{lead} + V_f \times I_f \times C_c \times R_{th(real)} \rightarrow R_{th(apparent)}
\]
The test results showed the difference about 10°C.
In “Vf-Tj method” it is necessary to obtain first the "Vf-Tj characteristics” which is practically linear as shown below. The formula to show the characteristics will change by an individual diode and the forward current applied.

An example of Vf-Tj characteristics:

\[ Tj = -885.52 \times Vf + 407.95 \]
Conclusion

After my proposals in Loughborough meeting (Spring 2015),

Procedure 1 (Tj method) was rejected from IEC 61215 and/or 61646.

Procedure 2 (Vf-Tj method) was remained in IEC 61215 and/or 61646.
This work was performed in cooperation with ONAMBA, Sanken Electric, SOMA Optics, Kyocera and SHARP.

I would particularly like to thank Dr. Paul Robust, Dr. Vivek Gade and Dr. Kent Whitfield.
Thank you for your attention.