Degradation Mechanisms of c-Si PV Cells Exposed to Acetic Acid Vapor

Tadanori Tanahashi, Norihiko Sakamoto, Hajime Shibata, Yukiko Hara, and Atsushi Masuda (AIST)
EL Images of c-Si PV Modules Exposed in Identical Outdoor Site (ca. 30 Years)

Mfg. in 1983

Pmax: -40.5%
Isc: -19.0%
Voc: -1.2%
FF: -25.6%
(vs. Name Plate)

Mfg. In 1984

Pmax: -43.9%
Isc: -9.5%
Voc: -0.6%
FF: -31.7%
(vs. Name Plate)
Background

Proposed Current Transport Mechanisms in Silver Contact\(^1\)

Field Emission (FE)

\[ N_D \geq 10^{20} \text{ cm}^{-3} \]

Thermionic Field Emission (TFE)

\[ 10^{17} \text{ cm}^{-3} < N_D < 10^{20} \text{ cm}^{-3} \]

Electron Tunneling

through glass layer

(directly or via nano-Ag colloids)

Dissolution of Glass-Silver Boundary Layer by Acetic Acid\(^2\)


EVA is Roughly Equivalent to ~1% Acetic Acid

0% Acid

20% Acid

1% Acid (pH~3)

All Samples Exposed for 1000 h at 85 °C.

In a PV package with EVA, PV materials are exposed to a very corrosive environment.

M. Kempe, Effects of Encapsulant Choice on Corrosion in PV Modules, SOPHIA Workshop PV-Module Reliability (2013)
Experimental Setup (HAc = Acetic Acid)

a) Experimental Setup

b) Hung PV cells

c) Setups in Oven

Thick Glass Chamber for Thin Layer Chromatography

PV cell

Saturated KCl aq. soln. +/- HAc (3%)
Flash IV Characteristics

IV Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>RT</th>
<th>85°C/80% rh</th>
</tr>
</thead>
<tbody>
<tr>
<td>P&lt;sub&gt;max&lt;/sub&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;sc&lt;/sub&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;oc&lt;/sub&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

% Change of IV Parameters

48 h Exposure

IV Curves

Current (A) vs. Voltage (V)

- 0 h
- 6 h
- 9 h
- 12 h
- 24 h
- 36 h
- 48 h

in HAc Vapor at 85°C/80% rh

RT

85°C

85°C/80% rh
EL & Quasi-Rs Images

Exposure to HAc Vapor at 85°C/80% rh

6 h

9 h

12 h

24 h

36 h

Quasi-Rs Map (36 h)
SEM / EPMA Images

Control

exposed to HAc Vapor

Pb

Pb
AC Impedance Characteristics in PV Cells / Modules

Fig. 3. Impedance loci of a PV module at low ($V_1$), intermediate ($V_2$) and high ($V_3$) reverse bias voltages.

Evolution of AC Equivalent Circuit to Confirm the Formation of Gap underneath Finger Electrodes
AC Impedance Characteristics Exposure to HAC Vapor at 85°C/80% rh
AC Impedance Characteristics

Exposure to HAc Vapor at 85°C/80% rh

Control (85°C/80% rh)
AC Impedance Characteristics Exposure to HAc Vapor at 85°C/80% rh

(a) Log-log plot of impedance magnitude (|Z|) and phase angle (θ) versus frequency. Black dots represent 0 h exposure, and orange dots represent 48 h exposure. Graphs show the effect of exposure on impedance characteristics.

(b) Equivalent Circuit Diagram:
- R1, R2, R3, L4
- C2, C3, C4
- Z2, Z3, Z4

(c) Real part of impedance (Z_re) graph with data points and lines representing different circuit configurations:
- 0 h: Data Point
- 48 h: Data Point
- R1 + Z2
- R1 + Z2 + Z4
- R1 + Z3
- R1 + Z2 + Z3
- R1 + Z2 + Z3 + Z4

Research Center for Photovoltaics
AC Impedance Characteristics

Exposure to HAc Vapor at 85°C/80% rh

Real Z (ohm)

Im. Z (ohm)

9 h
18 h
24 h
36 h
AC Impedance & IV Parameters

at 85 °C/80% rh

- C3
- C2

R3
R1
Isc
FF
Pmax

at 75 °C/80% rh

- C3
- C2

R3
R1
Isc
FF
Pmax

at 65 °C/80% rh

- C3
- C2

R3
R1
Isc
FF
Pmax
4 Parameter Logistic Model

\[ y = \frac{a - d}{1 + (x/c)^b} + d \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Phase I</th>
<th>Phase II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pmax</td>
<td>0.347</td>
<td>0.629</td>
</tr>
<tr>
<td>FF</td>
<td>0.376</td>
<td></td>
</tr>
<tr>
<td>Isc</td>
<td>0.547</td>
<td>0.588</td>
</tr>
</tbody>
</table>

Inflection Time (h)

Normalized Pmax

\[ \text{Normalized Pmax} = \frac{P_{\text{max}}}{P_{\text{max}} @ \text{Phase II}} \]

Exposure Time (h)
Putative Degradation Process on c-Si PV Cells Exposed to HAc

Finger Electrode  Emitter (Si)  Ag Pillar

Phase I  FF Decreasing  Phase II  $I_{sc}$ Decreasing

“Constellation” on PV Cell: Bright Spots are Only on Finger Electrodes
DH Stress Test of PV Module

DH Stress Test at 85°C/85% rh

- $R_1$
- $R_3$
- $C_2$
- $C_3$

% Change of PV Parameters

- Voc
- Isc
- FF
- Pmax

2500 h
2754 h

150805_01M
DH Stress Test of PV Module

2006 h

2500 h

2754 h

2837 h

2999 h

3510 h
Fig. 2. Alternative equivalent circuit with multiple diodes, resistances in series with each diode, and an outer shunt resistance.

Microelectronics Reliability 51 (2011) 2044–2048

150707_10: Exposure to HAc Vapor at 85/80
Evolution of Series Resistance (Rs) in DC Eq. Circuit

- **Finger electrode**
- **Emitter (Si)**
- **Ag Pillar**

**Phase I**
- **FF decreasing**

**Phase II**
- **I_{sc} decreasing**

**Graphs**
- **Resistance (ohm)**
  - at 85 °C
  - at 75 °C
  - at 65 °C

- **IV curve parameters normalized to initial value**
  - **I_{sc}**
  - **FF**
  - **P_{max}**

**Duration (h)**

**Legend**
- **Rs (dark IV)**
- **R1**
- **R3**
IV Characteristics of Bare PV Cells Exposed to HAc Vapor at 85 °C /80% rh

[Graph showing IV characteristics with various exposure times (0 h, 12 h, 24 h, 36 h, 60 h, 96 h) and a circuit diagram with Rs and Rsh]
Effects of DC Bias on $R_2 / C_2$ in Bare PV Cell Exposed to HAc Vapor at 85°C / 80% rh
Effects of DC Bias on $R_1 / R_3$ in Bare PV Cell Exposed to HAc Vapor at 85°C / 80% rh
Effects of DC Bias on $C_3$ in Bare PV Cell Exposed to HAc Vapor at 85°C / 80% rh

- $C_2 \sim 2$
- $C_3 \sim 2_{12\,h}$
- $C_3 \sim 2_{24\,h}$
- $C_3 \sim 2_{36\,h}$
- $C_3 \sim 2_{60\,h}$
- $C_3 \sim 2_{96\,h}$

Circuit diagram:
- $R_1$
- $C_2$
- $R_2$
- $C_3$
- $R_3$

Graph:
- Applied DC Voltage (V) vs. $C^{-2}$
- Points for $12\,h$, $24\,h$, $36\,h$, $60\,h$, $96\,h$

- Lines for $C_2 \sim 2$
- $C_3 \sim 2_{12\,h}$
- $C_3 \sim 2_{24\,h}$
- $C_3 \sim 2_{36\,h}$
- $C_3 \sim 2_{60\,h}$
- $C_3 \sim 2_{96\,h}$
Putative Degradation Process on c-Si PV Cells Exposed to HAc

- **Finger Electrode**
- **Emitter (Si)**
- **Ag Pillar**

**Phase I**
- FF Decreasing

**Phase II**
- Isc Decreasing
Conclusions

in “Bare c-Si PV Cells” exposed to HAc vapor,

Power-Loss (2 Phase degradation)

Phase I  Rapid decline of $P_{max}$ & FF
Emergence of $C_3$ & $R_3$  <Capacitor Formation>

Phase II  Gradual reduction of $P_{max}$ & $I_{sc}$
< MIS-like Component Formation>

Independence of each phase <- Difference in $E_a$
Gap formation underneath finger electrodes
  = closely relate to emergence of $C_3$ & $R_3$

in “c-Si PV Modules” under Damp Heat Stress Conditions,
Similar power-loss behaviors to those in cells exposed to HAc vapor.
  Especially, Emergence of $C_3$ & $R_3$ was confirmed during extended DH test.

Electrical signals derived from the gaps would be a crucial “aging signature“ in c-Si PV modules installed in fields.
Thank You for Your Attention!

Thank You for Your Participation in SAYURI-PV 2016