Flex-Pass-Gate SRAM Design for Static Noise Margin Enhancement Using FinFET-Based Technology

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Outline

• Background

• Proposal of Flex-Pass-Gate SRAM
  – Memory cell
  – Operation in array

• Performance Estimation for hp-32-nm LSTP Applications
  – Pass gate design strategy
  – Static noise margin estimation
  – Variability tolerance

• Conclusion
Background – SRAM Yield

Conventional 6Tr-SRAM

Increased Variation

Vth Variation

Malfunctions!

Design Margin

Read Margin, RM

Write Margin, WM

Trade Off
Flex-Pass-Gate SRAM

Conventional

Fixed $V_{th,PG}$

$V_{th,PG}$ for Write

$V_{th,PG}$ for Read

Flex-PG

3T-FinFET

4T-FinFET
3-Terminal and 4-Terminal FinFETs

3T-FinFET

4T-FinFET

Y-X Liu et al., 2003IEDM, 2004EDL (AIST)
RM and WM Enhancement

• Using Dynamic $V_{G2}$ Control

**Diagram:**
- **Lowering $V_{G2}$:**
  - $V_{G2} = -0.5$
- **Raising $V_{G2}$:**
  - $V_{G2} = 1.0$

**Graph:**
- **Margins vs. $V_{G2}$**
  - RM
  - WM

**Equations:**
- $V_{G2,R}$
- $V_{G2,W}$
Cell Layout and Area Overhead

- PG(4T-FinFET)
- Selective Gate Separation
- Contact of Vth-Ctrl Line

120F²

3rd Layer (V_{th-Ctrl}, V_{DD}, V_{SS}, BL)
2nd Layer (WL)
1st Layer (Intra-Cell, not shown)

3 Metal Layers Enough for Interconnection
Selective Gate Separation

Etching Stopper

Fin

P.R.

Gate

BOX

sub

DG Separation by Etching-Back Process

Top View

Cross-Sectional View

Fin Top

Source

Side Wall

Gate1

Gate2

100nm

G1

G2

H_{Fin} = 100nm

T_{Fin} = 25nm

100nm

K. Endo et al., 2007 IEEE EDL (AIST)
Array Configuration

- Column-by-Column $V_{G2}$ Control
Read Operation

• Stable Read

Column Peripheral

Row Peripheral

PG: On, High Vth

WL

BL

BLB

V_{th-Ctrl}

V_{th-Ctrl}
Write Operation

• Fast/Stable Write

PG-Leakage Current Reduction
1. Negative Low-Level on WL
2. Thicker Second-Gate Oxide
Performance Estimation Model

- Technology assumption: hp-32-nm LSTP

Device Model

10-nm G-S/D Underlap + S/D Doping Profile ($\sigma = 3$ nm)

Simulated $I_D-V_G$ of 3T-FinFET

Drain Current ($\mu$A/\mu$m)

Gate Voltage (V)

|$V_{DD}| = 0.05, 1.0$ V

PMOS

NMOS

$\text{Gate1}$

$\text{Gate2}$

$L_G = 20$ nm

$t_{ox1} = 1.2$ nm

$t_{ox2}$: Variable

$t_{ox1} = t_{ox2}$
PG Design for Write Margin

**Graph: Write Margin vs. Second Gate Voltage for Write**

- **A:** $t_{ox2} = t_{ox1} \quad \Rightarrow \quad V_{G2,W}$
- **B:** $t_{ox2} = 2.5 \times t_{ox1}$
- **C:** $t_{ox2} = 4.0 \times t_{ox1}$
- **D:** $t_{ox2} = 7.0 \times t_{ox1}$

The diagram illustrates the relationship between the write margin (mV) and the second gate voltage for write, $V_{G2,W}$ (V). The graphs show how the write margin changes with varying $t_{ox2}$ compared to $t_{ox1}$, indicating that increasing $t_{ox2}$ results in a larger $V_{G2,W}$.
PG Design for Hold Margin and Leakage Current

Write Condition

A: $t_{ox2} = t_{ox1}$, $V_{G2,W} = 0.70 \text{ V}$
B: $t_{ox2} = 2.5t_{ox1}$, $V_{G2,W} = 0.85 \text{ V}$
C: $t_{ox2} = 4.0t_{ox1}$, $V_{G2,W} = 1.00 \text{ V}$
D: $t_{ox2} = 7.0t_{ox1}$, $V_{G2,W} = 1.25 \text{ V}$

Low Level of WL Signal, $V_{WL,L}$ (V)

PG Leakage Current ($\mu$A/\mu m)

Hold Margin (mV)

Ticker $t_{ox2} \rightarrow$ Less Leakage
PG Design for RM and Readout Current

Ticker \( t_{ox2} \rightarrow \text{Larger Current} \)

- **B:** \( t_{ox2} = 2.5t_{ox1} \)
- **C:** \( t_{ox2} = 4.0t_{ox1} \)
- **D:** \( t_{ox2} = 7.0t_{ox1} \)

Second Gate Voltage for Read, \( V_{G2,R} \) (V)

PG Readout Current (μA/μm)

Read Margin (mV)

- \( V_{WL,L} \)
- \( V_{WL,H} \)
- \( V_{WL,L} \)

\[ V_{DD} = 1.0 \text{ V} \]
Summary of PG Design

- Larger Readout Current
- Less Leakage Current

Thicker $t_{\text{ox2}}$

- Larger $V_{\text{G2}}$
  for Sufficient WM

Signal Levels for PGs with $t_{\text{ox2}} = 4.0 t_{\text{ox1}}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Low Level</th>
<th>High Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>WL Signal $V_{\text{WL}}$ (V)</td>
<td>$V_{\text{WL,L}} / -1.0$</td>
<td>$V_{\text{WL,H}} / 1.0$</td>
</tr>
<tr>
<td>$V_{\text{G2,R}}$ (V)</td>
<td>$V_{\text{G2,R}} / -1.0$</td>
<td>$V_{\text{G2,W}} / 1.0$</td>
</tr>
</tbody>
</table>
Additional Peripheral Circuits

- **Column Address**
- **Row Address**
- **Column Dec.**
- **WE**
- **LS**
- **MC**
- **WLs**
- **V_{th-Ctrl}**
- **BLs**
- Level Shifter

**Symbols and Voltages:**
- $V_{DD}$
- $V_{SS} [=0]$
Asymmetric-Oxide DG

STEM images of the fabricated independent double-gate 4T-FinFETs

Asymmetric-Oxide DG

Symmetric $t_{ox}$ 4T-FinFET

Asymmetric $t_{ox}$ 4T-FinFET

Y.X. Liu et al., 2006 IEDM, 2007 IEEE EDL (AIST)
Asymmetric-Oxide DG

$t_{ox1} = t_{ox2} = 1.7 \text{ nm}$

$L_g = 1 \mu m$

$t_{ox1} = 1.7 \text{ nm}$
$t_{ox2} = 3.4 \text{ nm}$

$V_D = 0.05 \text{ V}$

Symmetric $t_{ox} \ 4T$-FinFET

Asymmetric $t_{ox} \ 4T$-FinFET

Y.X. Liu et al., 2006 IEDM, 2007 IEEE EDL (AIST)
RM/WM Enhancement by Flex-PG

Both RM and WM are Enhanced

Nominal Margins
Variability in Vth

**Fluctuation Model**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Fluctuation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Length</td>
<td>Gaussian</td>
</tr>
<tr>
<td>Fin Thickness</td>
<td>$3\sigma = 0.2 , L_G$</td>
</tr>
<tr>
<td>Channel Dopant Number</td>
<td>Poisson  $\mu = N_{\text{chan}}$</td>
</tr>
</tbody>
</table>

Device-Level Variability Suppression by Using an Undoped Body

* Number of Samples: 200
Variability in RM and WM

- 70-mV Gain of Margin for $6\sigma$ Variation
- Comparable Margin for $6\sigma$ Variation

* Number of Samples: 100
Conclusion

• Flex-PG SRAM enhances both RM and WM independently.
• Asymmetric 4T-FinFET improves the performance of the Flex-PG SRAM.
• Flex-PG SRAM is applicable to hp-32-nm LSTP applications, with sufficient tolerance for 6-σ variability.