Performance Limit of Parallel Electric Field Tunnel FET and Improvement by Modified Gate and Channel Configurations

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Outline

Background
- Why tunnel FET (TFET)
- Parallel electric field TFET (PE-TFET)

Performance of PE-TFET
- Device fabrication
- Experimental results

Proposal of Synthetic electric field TFET (SE-TFET)
- Device fabrication
- Experimental results

Summary
Conventionally, $V_{dd}$ scaling causes a significant increase in $I_{off}$ due to the lower limit of SS (~60mV/dec.) $V_{dd}$ scaling without $I_{off}$ increase can be done by steepening the SS
Why tunnel FET?

**MOSFET**

- Carrier flow is determined by thermal-injection mechanism
- $SS > 60\text{mV/dec.}$

**Tunnel FET**

- Carrier flow is determined by BTBT transport mechanism
- $SS < 60\text{mV/dec.}$
Lateral & vertical TFETs

- Two TFET architectures

Lateral (conventional) TFET

Vertical (parallel electric field) TFET

BTBT is limited in interface

\[ \text{L}_{\text{OV}}: \text{Overlap length} \]

\[ \Rightarrow \text{Small } I_D \]

BTBT area is enlarged

Y. Morita et al., Jpn. J. Appl. Phys. 52, 04CC25 (2013)
Objective of this work

- Performance of the parallel electric field TFET (PE-TFET), relation between ON current and overlap length, is analyzed.

- Proposal of modified TFET architecture to improve electrostatics (Synthetic electric field TFET)
Performance of the PE-TFET
Fabrication of PE-TFET with epichannel

S/D first & "Junction-last" TFET process

- SOI mesa etching (a)
- P I/I (b)
- BF₂ I/I (c)
- Activation (1000 °C)

- Si epitaxial growth, high-k and gate (d)
- Gate stack etch
- Contact
- Sintering

(a) SOI mesa etching

(b) P ion implantation

(c) BF₂ ion implantation

(d) Si epitaxial growth, high-k and gate

(e) Gate stack etch

BF₂ ion implantation

SOI mesa etching
Operation of p- & n-PE-TFETs

I_D-V_G

EOT = 1.3 nm Lg = 1000 nm Lov = 150 nm

p-TFET

V_D = -1 V

n-TFET

V_D = 1 V

V_D = -0.2 V

SS_{min} = 112

V_D = 0.2 V

SS_{min} = 72

G

High-k

S

D

S

D

n-TFET

p-TFET

BOX
Effect of $L_{OV}$ increase

Relation between $I_D$ and $L_{OV}$

Confirming $I_D$ increase with increasing $L_{OV}$
ON current degraded at $L_{OV} > 1000$ nm
Effect of $L_{OV}$ increase

Analysis using a distributed-element circuit

In ideal case ($R_S \sim 0$), $i-v$ relation can be describes as,

\[
\begin{align*}
- \frac{dv(x)}{dx} &= R_c i(x) \\
- \frac{di(x)}{dx} &= G v(x)
\end{align*}
\]
Effect of $L_{OV}$ increase

Relation between $I_D$ and $L_{OV}$

$\tau = \sqrt{\frac{1}{GR_C}} \sim \sqrt{\frac{G}{R_C}} V_D$

Ideal case ($R_S = 0$)

Considering $R_S$

Upper limit of ON current! $\sim \sqrt{\frac{G}{R_C}} V_D$
Limit of drain current in PE-TFET

\[ I_{\text{ONMAX}} \sim \sqrt{\frac{G}{R_C}} V_D \]

--->> Self-voltage-drop effect in thin channel

Trade off
Enhancing G  <<<--> Reducing R_C

Balance between tunnel conductance and channel resistance is critical.
Proposal of modified TFET architecture
Proposal of synthetic electric field TFET

- Multiplication of lateral & vertical electric fields

(a) Lateral TFET

(b) Parallel electric field TFET

(c) Synthetic electric field TFET

(d) Ultrathin undoped channel

High-k
Fabrication of SE-TFET with epichannel

- Based on source/drain-first CMOS process
Device structures

- Small amount of defects at epitaxial channel/source interface
Operation mechanism

Conventional (lateral) TFET

SE-TFET

BTBT window

Top E-field

Side + Top E-fields
Simulation of electric field

- Electric field at edges is enlarged by SE-effect.
- Scaling of channel thickness and width enhances SE-effect

**Electric field distribution**

- Electric field (V/cm)
- $W_{CH} = 20\,\text{nm}$, $D_{EPI} = 10\,\text{nm}$
- $W_{CH} = 50\,\text{nm}$, $D_{EPI} = 50\,\text{nm}$
Impact of channel width

- Better performance in narrower channel device

![Graph showing $I_D$ vs $V_G$ for different channel widths and parameters.](image)

- $W_{CH} = 0.17 \, \mu\text{m}$
- $W_{CH} = 1 \, \mu\text{m}$
- $W_{CH} = 10 \, \mu\text{m}$

- $D_{EPI} = 10 \, \text{nm}$
- $V_D = -0.05 \, \text{V}$
- $L_{OV} = 400 \, \text{nm}$

- $SS_{MIN} = 52$

![Graph showing $SS_{MIN}$ vs $W_{CH}$ for different $D_{EPI}$ and $V_D$.](image)
- $I_D$ at $W_{CH} = 0$ corresponds to the edge current.

![Impact of channel width](image)

- $L_{OV} = 400$ nm
- $V_D = -1$ V
- $V_G = -2$ V

- $D_{Epi} = 10$ nm
- $0.1$ uA/um
- $D_{Epi} = 16$ nm
- $5.4 \times 10^{-3}$ uA/um
• Edge current is enhanced by $D_{EPI}$ scaling.

0.7 uA
0.2 uA

$L_{OV} = 400$ nm

$V_D = -1$ V
$V_G = -2$ V

$D_{EPI} = 10$ nm
0.1 uA/um

$D_{EPI} = 16$ nm

$5.4 \times 10^{-3}$ uA/um
Scaling of both $D_{\text{EPI}}$ and $W_{\text{CH}}$ enhance performance.

- $D_{\text{EPI}} = 16 \text{ nm}$
- 4 nm (Prediction)
- 10 nm

FinFET-like structure is better.
Performance of SE-tunnel FinFET

Significant performance

SS_{MIN} = 58, I_D = 4 \text{ uA/um} @ (V_G, V_D) = (-0.5, -0.2 \text{ V})

400 \text{ uA/um} @ (V_G, V_D) = (-2, -1 \text{ V})
Summary

Parallel electric field TFET
• Limit of ON current
• Balance between tunnel conductance and channel resistance is critical

Synthetic electric field TFET
• Scaling induced performance enhancement
• FinFET-like slim device is promising.
• Significant performance in small voltage
  \[ SS_{\text{MIN}} = 58, \quad I_D = 4 \text{ uA/um} @ (V_G, V_D) = (-0.5, -0.2 \text{ V}) \]
  \[ 400 \text{ uA/um} @ (V_G, V_D) = (-2, -1 \text{ V}) \]
• The concept can be applicable to Ge or III-V TFETs.
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Thank you for your kind attention.
Benchmark

Our data
(No strain, no Ge, no metal SD, only by device consideration)