Enhancing SRAM Performance by Advanced FinFET Device and Circuit Technology Collaboration for 14nm Node and Beyond

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Issues in SRAM Cell Scaling

- Rapid increase of stand-by leakage
- Yield reduction due to $V_{th}$ variation
FinFET SRAM

Merit of FinFET in SRAM Cell
✓ Short Channel Effect Immunity
✓ Less $V_{th}$ variability expected

Bulk planar MOSFET

Dopant atoms

FinFET

Undoped channel
FinFET exhibits the highest performance
Scaled SRAM is realized by multi-gate devices.
Fluctuation of $V_{\text{th}}$ exist even for the undoped channel FinFET.

Stability of the SRAM cell is reduced due to variability.
Device and Circuit Collaboration for the FinFET SRAM

1. Device Approach for Suppressing Variability
   - Variability Analysis
   - Variability Reduction Process

2. Circuit Approach for Enhancing SRAM Stability
   - Independent-DG FinFET
   - Flex-Vth SRAM, Flex-PG SRAM
   - Dynamic PG Control SRAM
   - Fin Height Control SRAM

3. Future Prediction by the Device and Circuit Technology Collaboration
Device Approach for Suppressing Variability
FinFET Variability Analysis

$V_{th}$ Variation Sources

- Fin thickness
- Gate length
- Gate WF
- Oxide Thickness Charge
- Fin channel
- Dopant number

$\Delta T_{Fin}$
$\Delta L_G$
$\Delta \Phi_m$
$\Delta Q_{ox}$
$\Delta N_A$
Analytical Method

Variance ($\sigma^2$) of $V_t$: sum of each component

$$\sigma_{V_t}^2 = \left( \frac{\partial V_t}{\partial Lg} \sigma_{Lg} \right)^2 + \left( \frac{\partial V_t}{\partial T_{fin}} \sigma_{T_{fin}} \right)^2 + \left( \frac{\partial V_t}{\partial T_{ox}} \sigma_{T_{ox}} \right)^2$$

- Dimension variation sources
- WFV+Qox source
- Dopant source

S. Ouchi et al. (AIST), IEDM 2008
T. Matsukawa et al. (AIST), VLSI 2009
Dimension variation sources are small.
Main component is gate-stack variation.

K. Endo (AIST), EDL 2010
Origin of the WFV

Plane TEM image of the TiN film

Orientation Dependent WF for TiN

- <100> 4.6 eV
- <111> 4.4 eV

✓ Grain size of MG’s is comparable to scaled $L_G$
✓ Grains with different orientation causes WFV
WFV Reduction by Channel Smoothing

Y.X. Liu, (AIST) VLSI, 2010, p.101

Nano Wet etching (NWE)  Avt: Slope of Pelgrom Plot

✓ WFV is reduced due to uniformly aliened metal
Reducing WFV: Amorphous Metal-Gate

TiN film (Ref.)
- Sputtering
- Ti target
- Ar/N₂ gas

XRD (post RTA)
- Si(200)
- TiN(200)
- TiN

Plane view TEM (post RTA)
- Poly-crystal

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TaSiN film
- Sputtering
- TaSi₂ target
- Ar/N₂ gas

XRD
- Si(200)
- N₂/Ar=4%

Plane view TEM
- Amorphous
- 20 nm

The FinFET with the TaSiN MG

Top view SEM (after spacer formation)

Fin channel cross section TEM

Gate cross section TEM

Conformal TaSiN MG is formed

Reduction of Vth Variation

TaSiN gate shows smallest $A_{Vt}$ of 1.34$mV_{\mu m}$

Benchmark of $A_{vt}$

References of $A_{vt}$

[1] AIST, 2009

Circuit Approach to Enhance SRAM Stability
Independent-DG (IDG) FinFET

- **Common-DG**: Fixed Vth
- **Independent-DG**: Variable Vth

\[
\log_2 I_d = V_{g1} - V_{th1} \\
\log_2 I_d = V_{g2} - V_{th2}
\]

Y. X. Liu et al. (AIST) IEDM 2003
IDG-FinFET Example

K. Endo et al. (AIST), IEEE EDL 2007
**IDG-FinFET CMOS Circuits**

**CMOS Inverter**

K. Endo (AIST), EDL 2007

**Flex-V\textsubscript{th} SRAM**

K. Endo (AIST), IEDM 2008
EDL 2009

**Flex-PG SRAM Dynamic PG Control**

S. O’uchi (AIST), CICC 2007
ESSCIRC 2010
IEDM 2008

K. Endo (AIST), ESSDERC2008
IEDM 2008

\(V_{\text{th}}\) control of all Tr.

Reduction of leakage current

\(V_{\text{th}}\) control of pass-gate

Enhancing SNM
Active and stand-by leaks are controlled with the same SNM
Flex-Pass-Gate (PG) SRAM Cell

Vth control of the PG enhances noise margin

S. O’uchi et al. (AIST), 2007 IEEE CICC

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**Flex-PG SRAM Cell Results**

**Read Margin**

- Flexible noise margin control is successfully demonstrated.
- Both RM and WM are enhanced.

K. Endo et al. (AIST), IEDM 2008, ESSDERC 2008
Dynamic PG Control Algorithm

\[ V_{VThCtrl} = V_{VThCtrl} + \Delta V \]

Start Read

Detect Data?

Pass

\[ V_{VTCtrl} = V_{VTCtrl,0} \]

Fail

\[ V_{VThCtrl} = V_{VThCtrl} + \Delta V \]

End Read

The optimal bias is found for each cell and the instability is avoided.

Read speed reduction is avoided.

S. O’uchi et al. (AIST), ESSCIRC 2010, 474
2 step read keeps 6-sigma tolerance of SNM

STEP 1

$V_{VtCtrl,0} = 0.25V$

$V_{VtCtrl} = 0.40V$

STEP 2

$L_g = 20nm$

$V_{DD} = 0.5V$

20-nm-$L_G$ technology

$V_{DD} = 0.5V$

$V_{VtCtrl} = 0.25V$

$V_{VtCtrl} = 0.40V$

Pass

Pass

(74%)

(26%)

S. O’uchi et al. (AIST), ESSCIRC 2010, 474
Fin Height Control SRAM

PD with a high-fin  PG with a low-fin

(a)  
Source  
Gate  
Sidewall  
Drain  

Source  
Gate  

tox = 2.3 nm  
Hfin = 91 nm  
n+-poly-Si  

(b)  

Source  
Gate  

n+-poly-Si  
TiN  
Tsi = 18 nm  

(c)  

n+-poly-Si  
TiN  
Tsi = 20 nm  

(d)  

Recessed active region

Fin height control enhances SNM

Y. Liu et al. (AIST), ESSDERC 2010

0 50 100 150 200 250 300

0 0.2 0.4 0.6 0.8 1 1.2

SNM [mV]  

VDD [V]  

All = high-fins, β = 1  
PG = low-fin, β = 2  
PG and PU = low-fins, β = 2  

Low-fin: Hfin = 45 nm  
High-fin: Hfin = 91 nm
Future Prediction by the Device and Circuit Technology Collaboration
Simulated SRAM Cell

✓ TaSiN amorphous metal-gate (A_{VT} 1.34)
✓ Flex-PG Technology for enhancing SNM

Monte Carlo SPICE simulation using the FinFET compact model for 14- and 10-nm technology

✓ Device parameters are from ITRS 2011
FinFET Compact Model (AIST)

T. Nakagawa, et al., (AIST), IWCM, 2008
Common-DG SRAM suffers form variability in spite of TaSiN MG
Simulated Results (10-nm Node)

Flex-PG and amorphous TaSiN enables 10-nm SRAM cell with sufficient margin.
Summary

✓ Reduction of the WFV has been successfully demonstrated.

✓ Independent-DG FinFET have been introduced into the SRAM cell to enhance performance.

✓ The device and circuit collaboration enables the 10-nm SRAM cell and beyond with sufficient margin.

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